

**REMARKS/ARGUMENTS**

The present application deals with a solution for determining the latch location of a stuck-at fault problem in a scan chain. While data cannot be transmitted down the scan chain through a stuck-at fault location, data in properly operating latches downstream of the stuck-at fault location can be shifted down the chain to the output. By varying or perturbing operating parameters such as power supply and reference voltages, clock timing patterns, temperature and timing sequences, one or more latches down the SRL chain from the stuck-at fault location may be triggered to change state from the stuck-at fault value. The SRL chain is then operated to shift data out the output of the SRL chain. The output is monitored and any change in value of a latch from the stuck-at state is noted as identifying all good latch positions from the changed latch to end of the chain. The perturbation process is repeated varying each of the selected operating parameters a number of times to locate the latch position following the stuck-at fault latch. This solution to the stuck fault problem:

1. Provides rapid on-the-fly diagnosis.
2. Pinpoints a defective SRL with high probability.
3. Is compatible with existing test methodologies and test systems.
4. Eliminates extensive test result data collection.
5. Provides relatively simple implementation.
6. Is easily simplified and automated for manufacturing test.
7. Provides a quick and direct path from test system to the solution.

**Claim Rejection Under 35 USC 103**

Original claims 1 to 8 were rejected under 35 USC 103(a) as being unpatentable over “A Technique for Fault Diagrams of Defects in Scan Chains” by Guo et al in view of IBM Technical Disclosure NN81081677.

The Examiner points out that Guo et al does not teach causing permutation in operating parameters, such as supply voltage reference voltage, timing pattern and temperatures to trigger a change in state of latches value and contends it is obvious to include the teaching of IBM publication NN81081677 to speed up overall test time. However, there is nothing in the IBM publication about triggering a change in state to introduce data into a inaccessible latches in a stuck-at fault LSSD chain. The purpose of the IBM publication technique is to determine levels that cause a failure not to introduce data to detect the position of an existing failure. Further, it would be obvious to those skilled in the art to substitute any teaching in the IBM publication for the ATPG techniques discussed in the Guo article. The Guo article on the first page points out problems with ATPG techniques then proceeds to use those techniques in its fault diagnosis of scan chains. The IBM publication was published years before the Guo article was written. If ATPG techniques are so disadvantageous and it was obvious to use the teaching of the IBM publication, for the purposes the Examiner proposes, the Guo article certainly would have used them. However, the IBM publication does not teach anything about triggering a change in state for the purpose of locating stuck-at fault bits and it would not be obvious to use the teachings of the IBM technical disclosure bulletin for the purposes not suggested therein.

All the claims are allowable over the prior art for the above reasons. Each of the independent claims call for permutation of certain operating parameters to introduce a change in operating states of memory units in a scan path with a stuck-at fault latch and using such a change to locate the stuck-at fault latch. The dependent claims contain limitations that further distinguish them from the prior art.

### **Rejection of Claims 4 and 8 under 35 USC 112**

Claims 4 and 8 have been amended so that they no longer contain reference to limitations without insufficient antecedent basis.

### **Objections to the Specification and Abstract**

The Abstract has been modified in light of the Examiner's remarks and the Specification has been changed in light of the Examiner's remarks except for 9a, 9c, 9d, 9e and 9f, which are correct as presented.

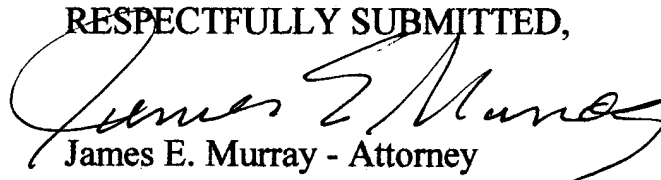
### **Objections to the Drawings**

The attached sheets of drawings have been modified in response to suggestions of the Examiner. For instance, Figure 1 now contains lines 104 between the SRLs 100; Figure 2 has been changed by adding the numeral "200" and changing the numeral "402" to -- 210 --; Figure 3 has been modified by changing the numeral "303" to -- 302 --; the spelling of "noise" has been corrected in Figure 5. Further reference to "SIS", "SRO", 604 and 608 have been added to the description. However, cell 308a is correctly numbered. Figure 4 was not changed

in that it correctly shows the operation of the circuit. Instead, the specification has been modified to cover the illustrated number string.

For the above reasons, it is respectfully submitted that all claims are allowable, and therefore it is requested that the application be reconsidered, allowed and passed to issue.

RESPECTFULLY SUBMITTED,

A handwritten signature in black ink, appearing to read "James E. Murray", is written over the printed name.

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Attachments: Replacement sheets for Drawings and the Abstract

## STUCK-AT SCAN CHAIN DIAGNOSTIC METHOD

### ABSTRACT

While data cannot be transmitted down a scan chain through a stuck-at fault location, data in properly operating latches downstream of the stuck-at fault location can be shifted down the chain. By varying operating parameters, such as power supply and reference voltages, clock timing patterns, temperature and timing sequences, one or more latches down the SRL chain from the stuck-at fault location may be triggered to change state from the stuck-at fault value. The SRL chain is then operated to shift data out the output of the SRL chain. The output is monitored and any change in value from the stuck-at state is noted as identifying all good latch positions to end of the chain. The process is repeated: varying each of the selected operating parameters until the latch position following the stuck-at fault latch is identified.